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EXAMINER	
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2816	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/683,552	STYDUHAR, MARK S.	
	Examiner	Art Unit	
	Hiep Nguyen	2816	MW

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-11 and 13-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-11 and 13-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

4 ☒ Specification pages 9-13

DETAILED ACTION

Claim Objections

Claims 4, 5 and 13 are objected to because of the following informalities: Claims 4, 5, 13 are objected to because they depend on cancelled claims.

Appropriate correction is required.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the recitation " a circuit for setting a trip point of a rising edge of an input signal" in claims 1 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities:

The disclosure [0011] is objected to because the input signal does not have " a trip point of a rising edge" and " a trip point of a falling edge". Only the device that receives the input signal can be set to have trip points in response to the rising edge and to the falling edge of the input signal.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 6 and 15 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The recitation wherein said input signal causes said comparator to appear as an asymmetric inverting Schmitt trigger" in claims 6 and 15, is not disclosed in the specification.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 4-11 and 13-20 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Correction and/or clarification is required.

Regarding claim 1, the recitation "a circuit for setting a trip point of a rising edge of an input signal" on lines 2 is indefinite because it is misdescriptive. The input signal does not have a trip point. Only the a device (comparator) can be set to have trip points in response to the rising edge and to the falling edge of the input signal by setting a value for the reference voltage or the W/L ratio of the transistors. The same analysis is true for the recitation " a trip point of a falling edge of said input signal" on lines 4-5. The recitation "wherein said comparator cycles between **an analog circuit** and **a digital circuit**" on line 6 is indefinite because it is misdescriptive. There are no **separate** "an analog circuit" and "a digital circuit". In fact, the "an analog circuit" and the "a digital circuit" is a same differential amplifier that has **two operating states**: analog and digital states depending on the input signal level with respect to the level of reference signal.

Regarding claims 5 and 14, the recitation " said digital circuit" is misdescriptive for the same reason mentioned in the rejection of claim 1.

Regarding claims 8 and 9, the recitation ""said **trip point** of a falling edge of **an input signal** increases by increasing said width-to- length ratio" is indefinite because it is misdescriptive. an input signal does not have a **trip point**. As understood by the examiner, the device that receives the input signal has a trip point. When the **level** of the input signal reaches the trip point of the device, the device is activated.

Regarding claim 10 the recitation "wherein said comparator cycles between **an analog circuit** and **a digital circuit**" on line 6 is misdescriptive for the same reason mentioned in the rejection of claim 1. The recitation " said trip point of a falling edge of **an input signal**" on lines 7 and 9 is indefinite because it is misdescriptive. The input signal **does not have a trip point**. Only a device (comparator) can be set to have trip points in response to the rising edge and to the falling edge of the input signal by setting a value for the reference voltage.

Regarding claim 16 the recitation "comprising **a first portion operatively connected** to **a second portion**" on lines 1-3 is indefinite because it is misdescriptive. As understood by the examiner, the comparator circuit **does not have two separate portions connected together**. In fact, the comparator is **a circuit** that has two operating modes depending on the level of the input signal. The applicant is requested to shows in the drawing **two separate circuits** (a first portion, a second portion) that are **operatively connected** in the drawing. The recitation "wherein said comparator cycles between **an analog circuit** and **a digital circuit**" on line 3 is misdescriptive for the same reason mentioned in the rejection of claim 1. It is not clear as to the "a first portion" and " a second portion" are the " an analog circuit" and the "a digital circuit". The recitation " a comparator for controlling **a trip point** of a rising and falling edge **of an input signal**" is indefinite because it is misdescriptive. The input signal does not have a trip point. Only the a device (comparator) can be set to have trip points in response to the rising edge and to the falling edge of the input signal by setting a value for the reference voltage or the W/l ratio of the transistors. The recitation " wherein said comparator controls a **delay between** rising and falling edge transition at an output signal of said comparator" on lines 4-5 is indefinite because it is not clear how the comparator can control a delay **between rising and falling edge** transition at an output signal of said comparator". The recitation " and wherein, said comparator controls a pulse width at said output signal of said comparator" is indefinite because it is misdescriptive. The reference voltage (Vref) is **constant** thus, the pulse width of the output signal is **not changed** unless the reference voltage (Vref) varies.

Claim 17 is indefinite because the recitation " said analog circuit" is misdescriptive. As discussed in the rejection of claim 1 and in the Response to Arguments, the " said analog circuit" **does not exist**. The "said analog circuit" is, in fact, **an operating state** of the comparator circuit

when the level of the input voltage is lower than the level of the reference signal. The recitation " a tail current source transistor **operatively** connected to said positive power supply" on line 7 is indefinite because it is misdescriptive. Figure 1 of the present application shows that the tail current source transistor is **directly** connected to said positive power supply (Vsup). As understood by the examiner the circuits of claims 16, 17 and 16,8 are the same circuit which presents two aspects of the circuit of figure 1. Depending on the level of the input signal, the circuit of figure 1 performs as an analog circuit or a digital circuit.

Claim 18 is indefinite because the recitation " said digital circuit" is misdescriptive. As discussed in the rejection of claim 1 and in the Response to Arguments, the " said digital circuit" **does not exist**. The "said digital circuit" is, in fact, an **operating state** of the comparator circuit when the level of the input voltage is higher than the level of the reference signal. The **analog circuit and the digital circuit** of claims 17 and 18 is, in fact, **one circuit that has two different operating modes ("analog" and "digital").** The applicant is requested to point out in the drawing two separate "analog circuit" and "digital circuit" that do not share the same components and that are "operatively " connected together.

Regarding claim 20, the recitation "wherein in **said digital circuit**, said input signal is at an input voltage **greater** than said positive external voltage reference" is indefinite because it is misdescriptive". If the input voltage is always **greater** than the positive external voltage reference, the output of the comparator never changes states. In other word, the comparator will not work properly. As understood by the examiner, when the level of the input signal is greater than the level of the positive external voltage reference, the output signal of the comparator changes state from low to high or from high to low and the comparator functions in a digital mode (or configuration). The recitation "said digital circuit" is misdescritive for the same reason raised above.

Claims 7, 11, 13 and 15 are indefinite because of the technical deficiencies of claims 1 and 10.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 5-7, 10, 11, 15 and 16, insofar as understood, are rejected under 35 U.S.C. 102(b) as being anticipated by Taguchi et al. (US Pat. 5,557,221).

Regarding claims 1 and 5 figure 9 of Taguchi shows a comparator comprising:

a circuit (Q301) for setting a trip point of a rising edge of " an input signal" according to a value of a positive external voltage reference (Vref =1.65V);

at least two transistors (Q302, Q305), in said circuit, for setting a trip point of a falling edge of " said input signal" according to the W/L ratio of said two transistors (see USP. 6,448,821, col. 3, lines 40-43; USP. 5,808,496 col. 3 lines 40-50);

wherein the comparator has two configurations: an analog configuration and a digital configuration depending on the level of the input signal with respect to the level of the reference signal. When the level of the input signal (Vin) is **below** the reference signal voltage applied to the input terminal (16), the comparator is in the **analog** configuration. When the input voltage (Vin) is **greater** than the reference (Vref) the comparator changes state, i.e., the output voltage of the comparator becomes high or low. This is the **digital** configuration of the comparator. There are no separate "analog circuit" and "digital" circuit " as recited.

Regarding claims 6 and 15, because the rising edge trip point and the falling edge trip point of the input transistors (Q301, Q302) can be set to have different values, the circuit appears to have hysteresis and when the falling edge of the input signal (Vin) goes down to the trip point of transistor (Q302), the output signal at the output terminal (20) changes state. Because of the different values of the rising edge trip point and the falling edge trip point, the output signal changes states at different levels of the input signal. Thus, the comparator functions as an asymmetric inverting Schmitt trigger.

Regarding claims 7 and 11, it is inherent that every transistor has W/L ratio and the switching threshold of the transistor depends on said mutual W/L ratio of transistors (Q302, Q305)(see USP. 6,448,821, col. 3, lines 40-43; USP. 5,808,496 col. 3 lines 40-50).

Regarding claims 8 and 9, it is inherent that the trip point of the falling edge of a transistor can be increased/ decreased by increasing/decreasing the W/L ratio (see USP. 6,502,223 col. 4, lines 5-10).

Regarding claim 10, figure 9 of Taguchi shows a comparator comprising:

a circuit (Q301) for setting a trip point of a rising edge of " an input signal" according to a value of a positive external voltage reference (Vref =1.65V);

at least two transistors (Q302, Q305), in said circuit, for setting a trip point of a falling edge of " said input signal" according to the W/L ratio of said two transistors (see USP. 6,448,821, col. 3, lines 40-43; USP. 5,808,496 col. 3 lines 40-50);

wherein the comparator has two configurations: an analog configuration and a digital configuration depending on the level of the input signal with respect to the level of the reference signal. When the level of the input signal (Vin) is **below** the reference signal voltage applied to the input terminal (16), the comparator is in the **analog** configuration. When the input voltage (Vin) is **greater** than the reference (Vref) the comparator changes state, i.e., the output voltage of the comparator becomes high or low. This is the **digital** configuration of the comparator. There are no separate "analog circuit" and "digital" circuit " as recited. The trip point of the falling edge of a transistor can be increased/ decreased by increasing/decreasing the W/L ratio (see USP. 6,502,223 col. 4, lines 5-10). The gate of the tail current source (Q305) is connected to the input signal thus the rise in the input signal switches the tail current transistor on.

Regarding claim 16, figure 9 of Taguchi shows a comparator for "controlling a trip point of a rising and falling edge of an input signal". The comparator has two configurations: an analog configuration and a digital configuration depending on the level of the input signal with respect to the level of the reference signal. When the level of the input signal (Vin) is below the reference signal voltage (Vref), the comparator is in the analog configuration. When the input voltage is greater than the reference voltage the comparator changes state, i.e., the output voltage of the comparator becomes high or low, the comparator is in the digital configuration . There is no "first portion" circuit operatively connected to "a second portion" circuit as recited. The output signal of the comparator is a square wave (well known) and the pulse width of the square wave depends on the rising edge trip point, the falling edge trip point and the level of the reference voltage of the comparator (well-known).

Claim 16, insofar as understood, is rejected under 35 U.S.C. 102(b) as being anticipated by Thiel (US Pat. 5.808,496).

Regarding claim 16, figure 1 of Theil shows a comparator for "controlling a trip point of a rising and falling edge of an input signal". The comparator has two configurations: an analog configuration and a digital configuration depending on the level of the input signal with respect to the level of the reference signal. When the level of the input signal is below the reference signal voltage applied to the input terminal (16), the comparator is in the analog configuration. When the input voltage at terminal (16) is greater than the reference at node (18) the comparator changes state, i.e., the output voltage of the comparator becomes high (Vsup) or low (ground). This is the digital configuration of the comparator. There is no "first portion" circuit operatively connected to "a second portion" circuit as recited. The output signal of the comparator is a square wave (well known) and the pulse width of the square wave depends on the rising edge trip point, the falling edge trip point and the level of the reference voltage of the comparator (well-known).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 17 and 18, insofar as understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Taguchi et al. (US Pat. 5,557,221).

Regarding claims 17 and 18, figure 9 of Taguchi shows a comparator circuit comprising:

an input signal terminal (Vin), an output signal terminal (20), e positive power supply voltage terminal (Vref), a tail current source transistor operatively connected to a positive power supply (Vcc), a first pair of transistors (Q301, Q302), a second pair of transistor (Q303, Q304)

which forms a current mirror and a inverter (365). Figure 9 of Taguchi does not show a plurality of inverters. However, it is old and well known in the art that an inverter is used to invert a signal and a plurality of inverters is used as a delay device. Therefore, it would have been obvious to those skilled in the art to replace the single inverter of Taguchi with a plurality of inverters for delaying the output signal of the comparator.

Regarding claims 19 and 20, the rise of the input signal (Vin) switches the tail current source transistor (Q305) and in the digital configuration, the input signal (Vin) is greater than the positive reference voltage (Vref).

Claims 4 and 13, insofar as understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Taguchi et al. (US Pat. 5,557,221) in view of Aspacio et al. (US Pat. 6,249,141).

Regarding claim 4 and 13, figure 9 of Taguchi includes all the limitations of claims 4 and 13 except for the limitation that there is a plurality of transmission gates in the circuit. Figure 5 of Aspacio shows a transmission gate implemented at the input of the circuit for controlling the flow of signal to the circuit. Therefore, it would have been obvious to those skilled in the art at the time the invention was made to implement a plurality of transmission gates to the circuit of Taguchi for controlling the flow of the signals in the circuit.

Claims 1, 4-11, 13-15 and 17-19, insofar as understood are rejected under 35 U.S.C. 103(a) as being unpatentable over Spitalny (5,574,401) in view of Manlove (5,498,986).

Regarding claim 1, figure 3 of Spitalny shows a comparator comprising:

a circuit (M1) for setting the rising edge trip point of the comparator according to an external voltage reference applied to the input terminal (22); and at least two transistors (M2,

M3) for setting the falling edge of the comparator according to the W/L ratio or the size of these transistors (see USP. 6,448,821, col. 3, lines 40-43; USP. 5,808,496 col. 3 lines 40-50); the comparator "cycles" between the analog configuration and the digital configuration depending on level of the input signal. When the level of the rising edge of the input signal (IN+) is lower than the level of the reference voltage and the level of the falling edge of the input signal is lower than the reference voltage, the comparator functions as **an analog circuit**. When the level of the rising edge of "the input signal" (IN+) is higher than reference voltage and the level of the falling edge of the input signal is higher than the reference voltage, the comparator functions as **a digital circuit**. The input (20) of the comparator is connected to the gate of the tail current source transistor (M3) thus, the rise in the input signal switches the tail current source transistor on. Figure 3 of Spitalny does not show that the reference voltage applied to the input terminal (22) is a positive voltage. Figure 3 of Manlove shows a comparator circuit (Q4, Q8, Q9) having a positive non-zero reference voltage (Vref) which is set close to ground to assure that the voltage potential at the comparator outputs (A, B) can swing far enough to assure that comparator output can swing rail-to ground under all process and temperature condition (col. 7, lines 43-48). Therefore, it would have been obvious to those skilled in the art at the time the invention was made to applied a positive non-zero reference voltage (Vref) to the input (22) to assure that the voltage potential at the comparator outputs can swing far enough to assure that comparator output can swing rail-to ground under all process and temperature condition. Note that the differential amplifier and the comparator circuits have the same structure and they function the same way.

Regarding claim 4, in the analog configuration, the comparator acts as a differential amplifier. Figure 3 of Spitalny does not show there is a plurality of transmission gates in the circuit. However, it is well known in the art that the transmission gates are used as **switches** that control the flow of current (signal) in a circuit. Therefore, it would have been obvious to those skilled in the art at the time the invention was made to implement transmission gates in the comparator circuit, for instance, to the input of the circuit to control the flow of the input signal to the circuit.

Regarding claim 5, when the input signal is greater than the positive external voltage, the output of the comparator switches state. Thus, it is in the digital configuration.

Regarding claim 6, because the rising edge trip point and the falling edge trip point of the input transistors (M1, M2) can be set to have different values, the circuit appears to have hysteresis and when the falling edge of the input signal (IN+) goes down the trip point of transistor (M2), the output signal at the output terminal (40) change state. Because of the different values of the rising edge trip point and the falling edge trip point, the output signal changes states at different levels of the input signal. Thus, the comparator functions as an asymmetric inverting Schmitt trigger.

Regarding claims 7, 8 and 9 it is inherent that transistors (M2) and (M3) can be set to have different lengths and widths (see Sakurai USP. 6,448,821, col. 3, lines 40-43) and from these different lengths and width, a width-to -length ratio can be formed and the trip point of the falling edge of an input signal can be increased or decreased by increasing or decreasing the W/L ratio.

Regarding claim 10, figure 3 of Spitalny shows a comparator comprising:

a circuit " for setting a trip point of a rising edge of an input signal" (M1) for setting the rising edge trip point of the comparator according to an external voltage reference applied to the input terminal (22); and

at least two transistors (M2, M3) for setting the falling edge of the comparator according to the W/L ratio or the size of these transistors (see Sakurai USP. 6,448,821, col. 3, lines 40-43); the comparator "cycles" between the analog configuration and the digital configuration depending on level of the input signal. When the level of the rising edge of the input signal (IN+) is lower than the reference voltage and the level of the falling edge of the input signal is lower than the reference voltage the comparator functions as "**an analog circuit**". When the level of the rising edge of the input signal (IN+) is higher than the reference voltage and the level of the falling edge of the input signal is lower than the reference voltage the comparator functions as "**a digital circuit**"(this is a basic operation of a comparator). The input (20) of the comparator is connected to the gate of the tail current source transistor (M3) thus, the rise in the input signal switches the tail current source transistor on. The trip point of the falling edge of "an input signal" can be changed (increase or decreased) by increasing/decreasing the width of the transistors, i.e., the W/L ratio.

Regarding claim 11, it is inherent that transistors (M2) and (M3) can be set to have different lengths and widths (see Sakurai USP. 6,448,821, col. 3, lines 40-43) and from these different lengths and width, a width-to -length ratio can be formed and the trip point of the falling edge of an input signal can be increased or decreased by increasing or decreasing the W/L ratio.

Regarding claim 13, in the analog configuration, the comparator acts as a differential amplifier. Figure 3 of Spitalny does not show there is a plurality of transmission gates in the circuit. However, it is well known in the art that the transmission gates are used as switches that control the flow of current (signal) in a circuit. Therefore, it would have been obvious to those skilled in the art at the time the invention was made to implement transmission gates in the comparator circuit, for instance to the input of the circuit, to control the flow of the input signal to the circuit.

Regarding claim 14, when the input voltage applied to terminal (20) is greater than the positive external voltage applied to terminal (22) the output of the comparator changes state and it performed as a digital circuit.

Regarding claim 15, because the rising edge trip point and the falling edge trip point of the input transistors (M1, M2) can be set to have different values, the circuit appears to have hysteresis and when the falling edge of the input signal (IN+) goes down the trip point of transistor (M2), the output signal at the output terminal (40) change state. Because of the different values of the rising edge trip point and the falling edge trip point, the output signal changes states at different levels of the input signal. Thus, the comparator functions as an asymmetric inverting Schmitt trigger.

Regarding claims 17-19, figure 3 of Spitalny shows a comparator having an analog configuration ("analog circuit") and a digital configuration ("digital circuit"). In other word claims 17 and 18 recite a same circuit. The comparator comprises:

an input signal (20), an output signal (40);

a positive power supply voltage terminal (Vdd);

a tail current transistor (M3) operatively connected to said positive power supply voltage terminal (Vdd) and said input signal terminal (20);

a first pair of transistors (M1, M2);

a second pair of transistors (M11, M12);

an external voltage reference terminal (22);

in the analog configuration, the input signal switches the tail current source transistor because the gate of the input transistor (M1) is connected to the gate of the tail current transistor (M3). Figure 3 of Spitalny does not show that the reference voltage applied to the input terminal (20) is a positive voltage. Figure 3 of Manlove shows a comparator circuit (Q4, Q8, Q9) having a positive non-zero reference voltage (Vref) which is set close to ground to assure that the voltage potential at the comparator outputs (A, B) can swing far enough to assure that comparator output can swing rail-to ground under all process and temperature condition (col. 7, lines 43-48). Therefore, it would have been obvious to those skilled in the art at the time the invention was made to applied a positive non-zero reference voltage (Vref) to the input (22) to assure that the voltage potential at the comparator outputs can swing far enough to assure that comparator output can swing rail-to ground under all process and temperature condition Note that the differential amplifier and the comparator circuits have the same structure and they function the same way.

Claim 17 and 18, insofar as understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over Thiel (US Pat. 5,808,496) in view of Manlove (5,498,986).

Regarding claims 17 and 18, figure 1 of Theil shows a comparator having an analog configuration ("analog circuit") and a digital configuration ("digital circuit"). In other word claims 17 and 18 recite **a same circuit**. The comparator comprises:

an input signal terminal (16), an output terminal (20);

a positive power supply voltage terminal (44);

an external power voltage reference terminal (18);

a tail current source transistor (30);

a first pair of transistors (22, 24);

a second pair of transistors (26, 28); and

a plurality of inverters (34, 38, 42).

Note that transistors that transistors (34, 38, 42) perform as inverters. When the inputs (gates transistors 34, 38, 42) are pulled high, the outputs (drains) of these transistors are pulled low and vice versa. The current mirror comprises transistors (26) and (28). Figure 1 of Thiel does not that the reference voltage is a positive voltage. Figure 3 of Manlove shows a comparator circuit (Q4, Q8, Q9) having a positive non-zero reference voltage (Vref) which is set close to ground to assure that the voltage potential at the comparator outputs (A, B) can swing far enough to assure that comparator output can swing rail-to ground under all process and temperature condition (col. 7, lines 43-48). Therefore, it would have been obvious to those skilled in the art at the time the invention was made to applied a positive non-zero reference voltage (Vref) to the input (18) to assure that the voltage potential at the comparator outputs can swing far enough to assure that comparator output can swing rail-to ground under all process and temperature condition. Note that the differential amplifier and the comparator circuits have the same structure and they function the same way.

Regarding claim 20, in the digital configuration, when the input voltage is greater than the positive external voltage reference, the output of the comparator changes state to a high/low level. This is a basic operation of a comparator when the input voltage level is greater than the reference voltage.

Response to Arguments

In the remarks Applicant state that the notation "I^1/4s" cannot be found in the entire specification. Attached are pages 9-13 wherein the notations "I^1/4s" and "I^1/4m" are widely used. The applicant is requested to read carefully these attached papers and to correct the specification accordingly.

In page 12, the Applicant states that the "analog circuit" which is the "first portion" is shown in figures 3 and 4. The "digital circuit" which is the "second portion" is shown in figure 5 and 6. As understood by the examiner, figures 3-6 represent a circuit of a comparator comprising a differential amplifier for comparing an input signal with a reference signal and output buffers (INV3, INV4).

As understood by the examiner, figures 3-6 shows a comparator circuit which has two states: "analog" and "digital" states depending on the level of the input signal with respect to the

reference voltage. In the **"analog"** state, the input voltage does not reach the level of the reference voltage, the transistors of the differential amplifier **partially** conduct current (in the **linear** mode). In the **"digital" mode**, the input voltage is equal or greater than the reference voltage, the transistors are in **saturation** mode. There are **no separate** "analog circuit" and "digital circuit" but **different operating modes** ("analog" and "digital") of the comparator circuit depending on the level of the input voltage with respect to the level of the reference voltage. Therefore, figures 3-6 represent a circuit of a comparator which operates in different modes.

In the Remarks, page 13, lines 18-34 and in page 14, lines 1-6, the applicant cites a paragraph in the specification stating that in the "**analog configuration**", there are static DC current paths present and certain transistors operate in the region known as **saturation**" and "in the **digital configuration**, static DC current paths are absent and the transistors are either operating in the **linear** (triode) region or cutoff region". These statements are **wrong** because it is well known in the art that in a **digital configuration**, the transistors of the circuit operate in **saturation region** and in the **linear configuration**, the transistors of the circuit operate in the **linear region.** In other word, in the digital configuration, **there is static DC current flowing** and the transistors are operating in the **saturation mode**. In the **analog configuration**, there is **no static DC current** flowing and the transistors are operating in the **linear region**. The applicant is requested to correct the specification accordingly.

Regarding 112, 2nd rejection, the applicant fails to clarify the recitation "said comparator **cycles** between an analog circuit and a **digital circuit**". The applicant states that the "first portion" is shown in figures 3 and 4 and the "second portion" is shown in figure 5 and 6. As discussed above, the comparator in figures 3-6 comprises a differential amplifier (a comparator that compares an input signal with a reference signal) and output buffers. The output of the differential amplifier is a digital signal and this digital signal is buffered by two inverters (INV3, INV4) thus there is no **cycling** " between an **analog circuit** and a **digital circuit**". The "analog circuit" and "digital circuit" are, in fact, **a same circuit** that has two different states (analog and digital) depending on the level of the input signal.

Regarding the prior art rejection, in pages 15 and 16 of the remarks, the applicant states that Thiel's circuit does not show **cycling** between an **analog and digital circuit**". As discussed

above, **there is no separate analog and digital circuit**". There are only **two states** of the comparator: analog and digital states. The "analog circuit" and the "digital circuit" **do not exist**. Howerever, the circuit of Thiel comprises the circuit of claims 16 and 17.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Hiep Nguyen whose telephone number is (703) 305-0127. The examiner can normally be reached on Monday to Friday from 7:30 A.M.to 4:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (703) 308-4876. The fax phone number for this Group is (703) 308-6251.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

Hiep Nguyen

01-05-03

TUAN T. LAM
PRIMARY EXAMINER